

WHAT IS CLAIMED IS:

- 1 1. An integrated circuit comprising:
2 an active termination circuit having first and second transistors of opposite type coupled
3 in series between a Vdd node of a first source potential and a Vss node of a second source
4 potential, the second source potential being lower than the first source potential, the at least one
5 termination node being coupled to a common node between the first and second transistors; and
6 a control circuit operable to bias the first and second transistors.
- 1 2. The integrated circuit as in claim 1 wherein the control circuit is operable to bias the first
2 and second transistors such that they provide a clamping function at the common node.
- 1 3. The integrated circuit of claim 1 wherein the first transistor is a MOSFET of the N-
2 channel type and the second transistor is a MOSFET of the P-channel type;
3 the drain of the first MOSFET is coupled to the Vdd node, and the drain of the second
4 MOSFET is coupled to the Vss node; and
5 the sources of both MOSFETs are coupled together and to the common node.
- 1 4. The integrated circuit of claim 1 wherein:
2 the control circuit includes a first control terminal control circuit operable to provide
3 a first control terminal drive signal to a control terminal of the first transistor, and a second
4 control terminal control circuit operable to provide a second control terminal drive signal to a
5 control terminal of the second transistor; and
6 the first and second control terminal drive signals are such that a quiescent voltage
7 potential of the common node is between the Vdd and Vss potentials.

1 5. The integrated circuit of claim 4 wherein the quiescent voltage potential of the
2 common node is at about a midpoint between the Vdd and Vss potentials.

1 6. The integrated circuit of claim 4 wherein the first and second control terminal control
2 circuits are operable to provide a first control terminal drive signal to a control terminal of
3 the first transistor and a second control terminal drive signal to a control terminal of the
4 second transistor to control the quiescent switch current through the first and second
5 transistors.

1 7. The integrated circuit of claim 4 wherein the first control terminal drive signal to a
2 control terminal of the first transistor and the second control terminal drive signal to a control
3 terminal of the second transistor are preferably controlled such that the quiescent current
4 conducted through the switch is substantially less than the current through two resistors whose
5 parallel resistance approximates the characteristic impedance of a coupled transmission line.

1 8. The integrated circuit of claim 4 wherein the device geometries, device size, and
2 processing of the first and second transistors are scaled so that they achieve a controlled
3 impedance and a quiescent voltage potential at the common node in response to an induced
4 voltages produced by the driver circuit coupling communication signals to the termination
5 node, and the quiescent voltage potential is at about a midpoint between the Vdd and Vss
6 potentials.

1 9. The integrated circuit of claim 4 wherein the first and second control terminal control
2 circuits are operable from voltage sources that are greater than the source potential Vdd for the
3 first control terminal control circuit, and less than the source potential Vss for the second

4 control terminal control circuit, and are capable of providing control terminal control signals,
5 respectively, that are greater than the source potential V_{dd} and less than the source potential V_{ss} .

1 10. The integrated circuit of claim 1 and further comprising:
2 a third transistor having a current path and a control terminal, the current path coupled
3 between the first transistor and the voltage source V_{dd} ; and
4 a fourth transistor, having a current path and a control terminal, the current path coupled
5 between the second transistor and the voltage source V_{ss} wherein the operation of the first and
6 second transistors can be selectively enabled or disabled by control signals coupled to the control
7 terminals of the third and fourth transistors.

1 11. The integrated circuit of claim 10 wherein the third transistor is a P-channel MOSFET
2 and the fourth transistor is an N-channel MOSFET.

1 12. The integrated circuit of claim 1 wherein the control terminal control circuit preferably
2 includes a fifth transistor and a sixth transistor in series across a V_{dd} node of a first source
3 potential and a V_{ss} node of a second source potential and scaled to the first and second
4 transistors; and
5 a current source coupled to at least one of the fifth or sixth transistor that controls the
6 quiescent current level in the first and second transistors.

1 13. The integrated circuit of claim 12 wherein the fifth transistor is an N-channel MOSFET,
2 and the sixth transistor is a P-channel MOSFET.

1 14. The integrated circuit of claim 1 wherein the control circuit preferably includes a voltage
2 source operable to produce a voltage potential of about a midpoint of the voltages of the voltage
3 sources Vdd and Vss.

1 15. The integrated circuit of claim 1 wherein the control circuit preferably includes a voltage
2 source operable to produce a voltage potential responsive to an externally supplied input voltage.

1 16. The integrated circuit of claim 1 and further comprising a resistor coupled between
2 the common node and the termination node.

1 17. An active termination circuit, comprising:
2 a first MOSFET having a gate terminal, a drain terminal, and a source terminal, the
3 source terminal coupled to a common node, and the drain terminal coupled to a Vdd node of
4 a first source potential;
5 a second MOSFET having a gate terminal, a drain terminal, and a source terminal, the
6 source terminal coupled to the common node, and the drain terminal coupled to a Vss node
7 of a second source potential, the second source potential being lower than the first source
8 potential; and
9 a control circuit operable to bias the first and second MOSFETs.

1 18. The active termination circuit of claim 17 wherein the control circuit operates to bias the
2 first and second MOSFETs such that they exhibit a controlled impedance at the common node.

1 19. The active termination circuit of claim 17, wherein the first MOSFET is an N-channel
2 MOSFET and the second MOSFET is a P-channel MOSFET.

1 20. The active termination circuit of claim 17, wherein the gate of the first MOSFET is
2 coupled to a voltage source between the Vdd and Vss potentials and the gate of the second
3 MOSFET is coupled to another voltage source of a lower potential.

1 21. The active termination circuit of claim 20, wherein the potential difference between the
2 voltage sources coupled to the gates of the first and second MOSFETs is controlled by a current
3 source.

1 22. The active termination circuit of claim 17 wherein the control circuit comprises:
2 a first operational amplifier with an output coupled to the gate terminal of the first
3 MOSFET; and
4 a second operation amplifier with an output coupled to the gate terminal of the second
5 MOSFET.

1 23. The active termination circuit of claim 22 wherein the first MOSFET is an N-channel
2 MOSFET and the second MOSFET is a P-channel MOSFET and wherein the first operational
3 amplifier is powered by a power supply potential greater than Vdd and the second operational
4 amplifier is powered by a power supply potential less than Vss, the first and second operational
5 amplifiers capable of producing gate drive signals greater than the power supply potential Vdd
6 and less than the power supply potential Vss, respectively.

1 24. The active termination circuit of claim 23 and further comprising:
2 a third MOSFET with a channel coupled between Vdd and the first operational amplifier,
3 the third MOSFET having a gate terminal coupled to the gate terminal of the first MOSFET, the
4 third MOSFET being an N-channel MOSFET; and

5 a fourth MOSFET with a channel coupled between Vss and the first operational
6 amplifier, the fourth MOSFET having a gate terminal coupled to the gate terminal of the second
7 MOSFET, the fourth MOSFET being a P-channel MOSFET.

1 25. The active termination circuit of claim 17 and further comprising a first enable switch
2 coupled between the first MOSFET and Vdd and a second enable switch coupled between the
3 second MOSFET and Vss.

1 26. An active termination circuit, comprising:

2 a first bipolar transistor having a base terminal, a collector terminal, and an emitter
3 terminal, the emitter terminal coupled to a common node, and the collector terminal coupled
4 to a Vdd node of a first source potential;

5 a second bipolar transistor having a base terminal, a collector terminal, and a emitter
6 terminal, the emitter terminal coupled to the common node, and the emitter terminal coupled
7 to a Vss node of a second source potential, the second source potential being lower than the
8 first source potential; and

9 a control circuit operable to bias the first and second bipolar transistors such that they
10 exhibit a controlled impedance at the common node.

1 27. A method of operating an active termination circuit, the method comprising:

2 biasing first and second series coupled transistors of opposite type such that they exhibit a
3 controlled impedance at a common node thereof, wherein the first and second transistors are
4 coupled in series across a Vdd node of a first source potential and a Vss node of a second source
5 potential, the common node being between the first and second transistors , and the second
6 source potential being lower than the first source potential.

1 28. The method of claim 27 wherein biasing first and second series coupled transistors
2 comprises producing first and second control terminal drive signals and applying said first and
3 second control terminal drive signal to the first and second series coupled transistors, the first
4 and second control terminal drive signals produced such that a quiescent voltage potential of the
5 common node is between the Vdd and Vss potentials.

1 29. The method of claim 28 wherein the first and second series coupled transistors are
2 MOSFETs.

1 30. The method of claim 27 wherein the quiescent voltage potential of the common node
2 is produced at about a midpoint between the Vdd and Vss potentials.

1 31. The method of claim 27 and further comprising scaling device geometries, device
2 size, and processing of the first and second MOSFETs so that their coupled sources produce
3 a controlled impedance and a quiescent voltage potential at the common node in response to
4 an induced voltages produced by the driver circuit coupling communication signals to the
5 termination node.